CLAIMS

1. A system for built-in test for a GPS receiver comprising:

a system processor;

a radio frequency (RF) input coupled to said system processor by a first operational signal path; and

a loop forward built-in test equipment (BITE) coupled to said system processor and to said RF input for providing an RF test signal to said RF input.

2. The system of Claim 1, further comprising:

a data output port coupled to said system processor by a second operational signal path; and

a loop backward built-in test equipment (BITE) coupled to said system processor and to said data output port for providing sampled output data to said system processor.

3. The system of Claim 1, wherein said operational signal path comprises an L1 signal path and an L2 signal path.

4. The system of Claim 1, wherein said loop forward BITE comprises a code generator for generating a test bit

sequence that emulates a set or subset of data in accordance with a GPS data message format.

5. The system of Claim 1, wherein said RF test signal is modulated using a code selected from the group consisting of pseudo M code, P code, and C/A code.

6. The system of Claim 1, wherein said first operational signal path comprises a Selective Availability/Anti-Spoof Module (SAASM).

7. The system of Claim 1, wherein said loop forward BITE is coupled to said RF input by a directional coupler.

8. A GPS receiver comprising:

an antenna input;

an analog processing block coupled to said antenna input;

a digital signal processor (DSP) coupled to said analog processing block;

a system processor coupled to said DSP; and

a loop forward built-in test equipment (BITE) coupled to said system processor and to said analog processing block for providing an RF test signal to said analog processing block.

9. The system of Claim 8, wherein said antenna input and said loop forward BITE are coupled to said analog processing block by a switch for selecting a signal from said antenna input or a signal from said loop forward BITE.

10. The system of Claim 8, wherein said loop forward BITE is coupled to said antenna input and said loop forward BITE are coupled to said analog processing block by a directional coupler.

11. The system of Claim 8, wherein said loop forward BITE comprises a code generator.

12. The system of Claim 11, wherein said code generator is a field programmable gate array (FPGA).

13. The system of Claim 11, further comprising an RF modulator for generating an RF carrier and modulating said carrier with a code generated by said code generator.

14. A method for performing built-in test (BIT) of a GPS receiver comprising:

generating a test data message within said GPS receiver;

generating a first RF carrier within said GPS receiver;

modulating said first RF carrier with said test data message to produce a first RF test signal; and

coupling said first RF test signal to an RF input of said GPS receiver.

15. The method of Claim 14, further comprising:

generating a second RF carrier within said GPS receiver;

modulating said second RF carrier with said test data message to produce a second RF test signal; and

coupling said second RF test signal to said RF input of said GPS receiver.

16. The method of Claim 15, wherein said first RF carrier and said second RF carrier have the same frequency.

17. The method of Claim 16, wherein said first RF carrier has a frequency that is different from the frequency of said second RF carrier.

18. The method of Claim 14, further comprising:

providing positioning data to an input/output (I/O) block for formatting;

transmitting said data over an output data port;

sampling the transmitted data at said output data port; and

comparing the transmitted data to the positioning data provided to the I/O block.

19. The method of Claim 18, wherein said positioning data is derived from a signal input to said RF input.

20. The method of Claim 18, wherein said positioning data is specifically generated for test purposes by a system processor.